

FIG 1A

Destination-Register	Source-Register 1	Source-Register 2	Mnemonic	0
kd-Bits	ks1-Bits	ks2-Bits	m-Bits	

Normal Commands

FIG 1B

Destination-Register	Source-Register 1	Source-Register 2	Mnemonic	Condition Flag
kd-Bits	ks1-Bits	ks2-Bits	m-Bits	p-Bits

Conditional Commands

FIG 1C

Destination-Flag	Source-Register 1	Source-Register 2	Mnemonic	0
p-Bits	ks1-Bits	ks2-Bits	m-Bits	

pxx Commands

FIG 1D

0	Source-Register 1	Source-Register 2	Mnemonic	0
	ks1-Bits	ks2-Bits	m-Bits	

loopxx-Commands

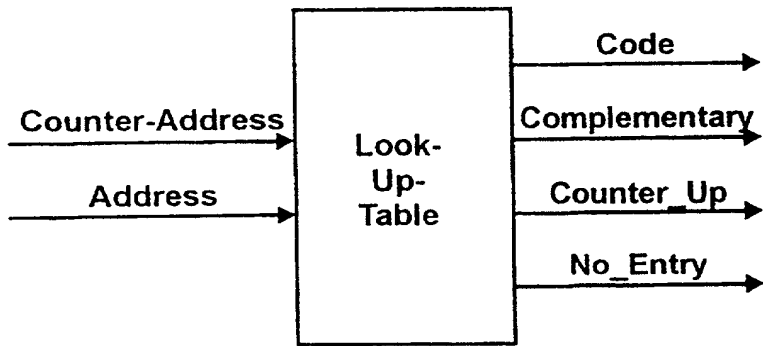


FIG 2

Config-Bits	Config-Index	Part-Number	Comple-mentary	Counter_Up	No_Entry
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FIG 3A

0	0	0	0	0	1
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FIG 3B

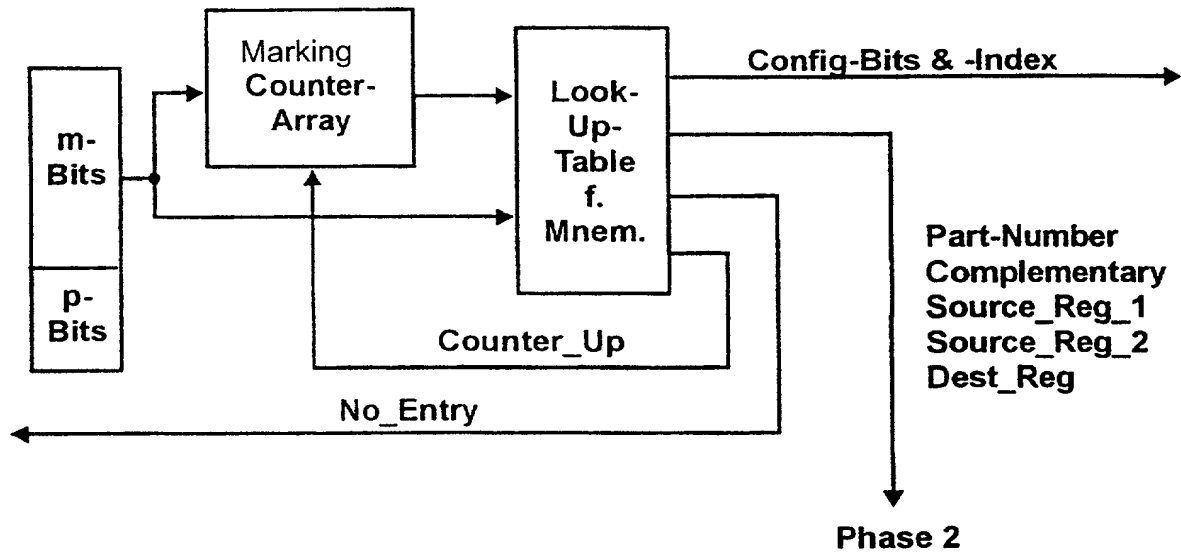


FIG 4

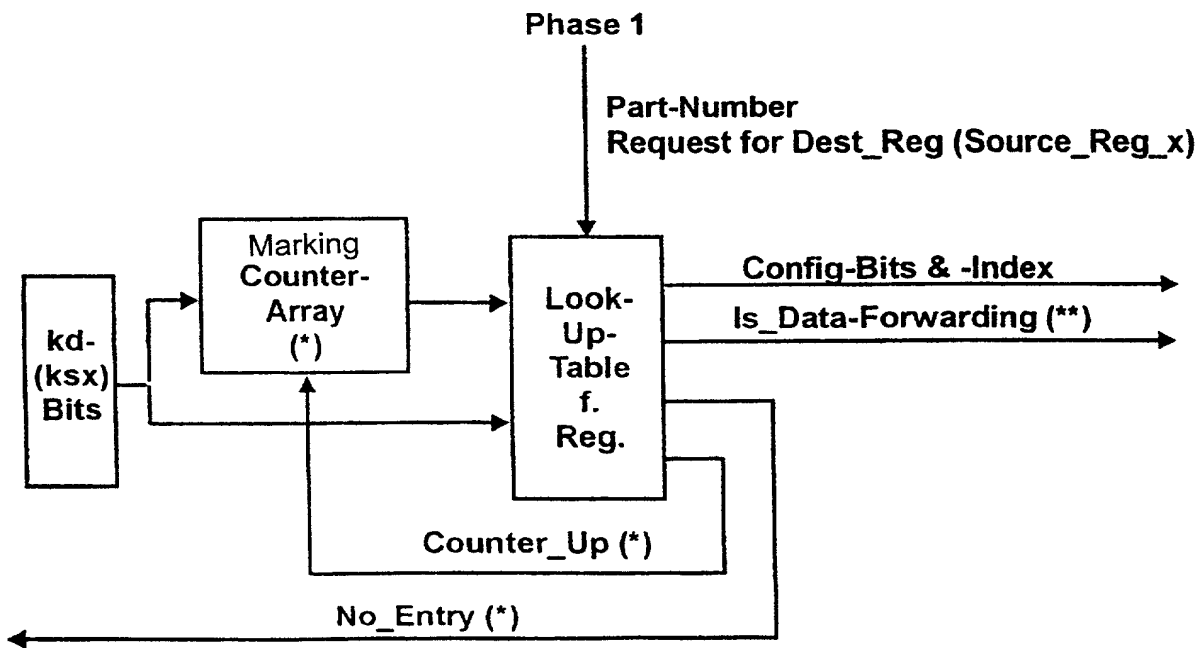


FIG 5

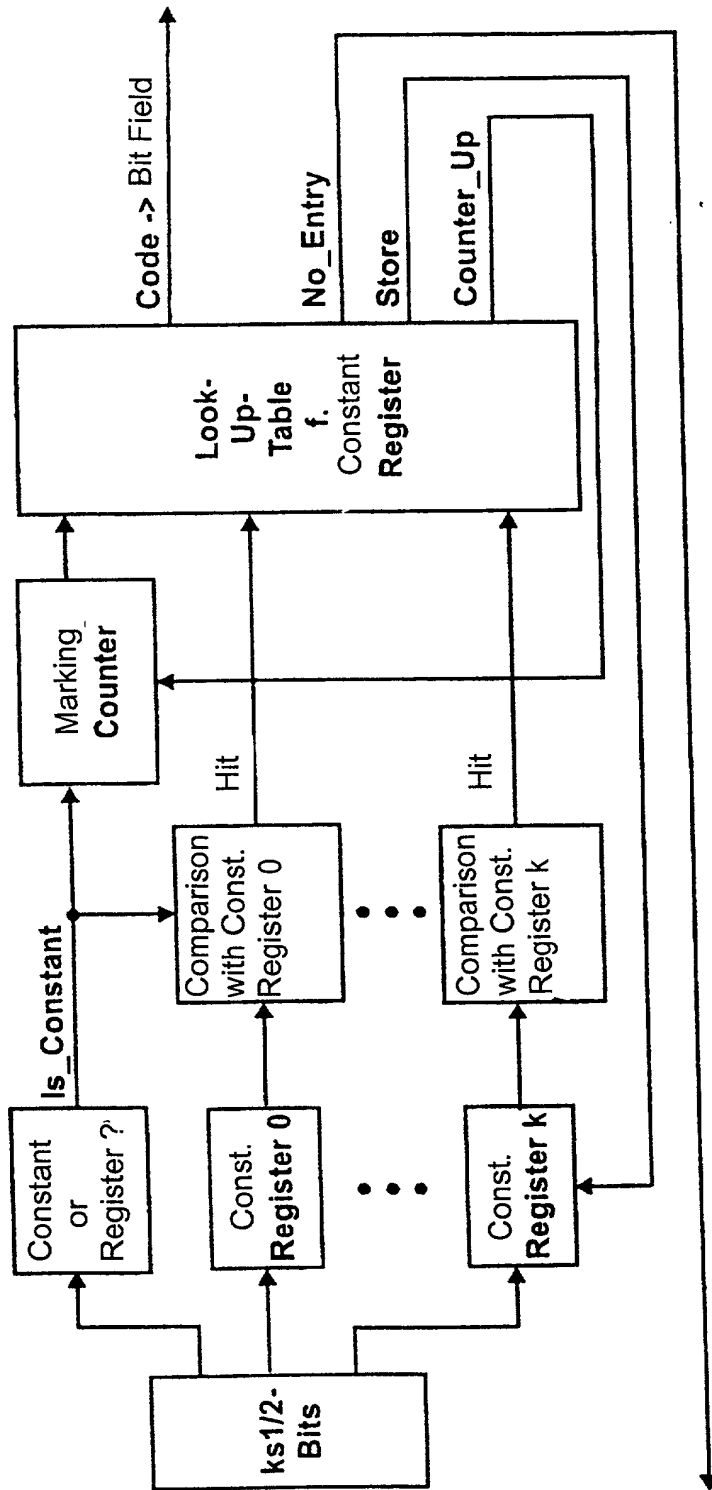


FIG 6

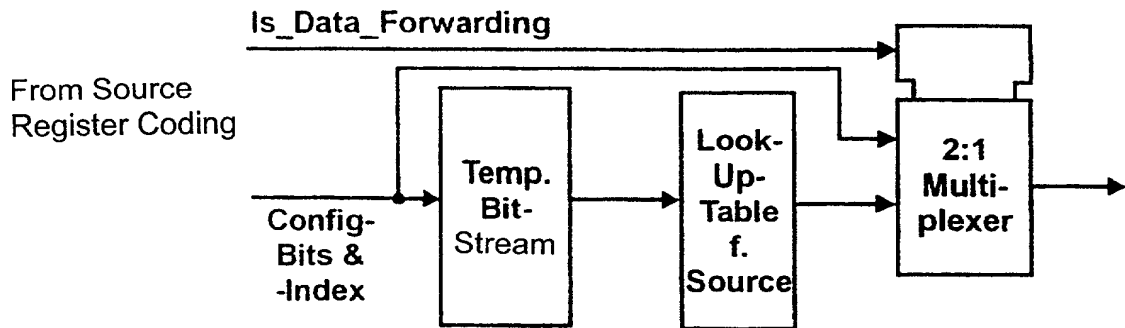


FIG 7

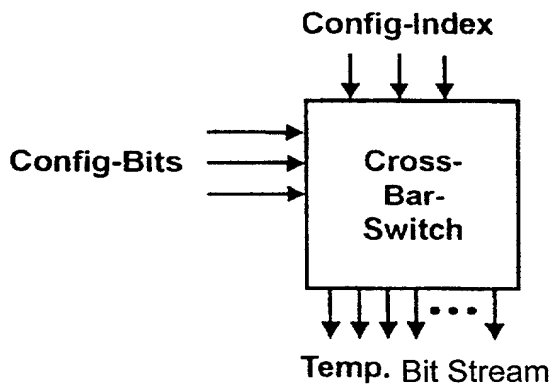


FIG 8

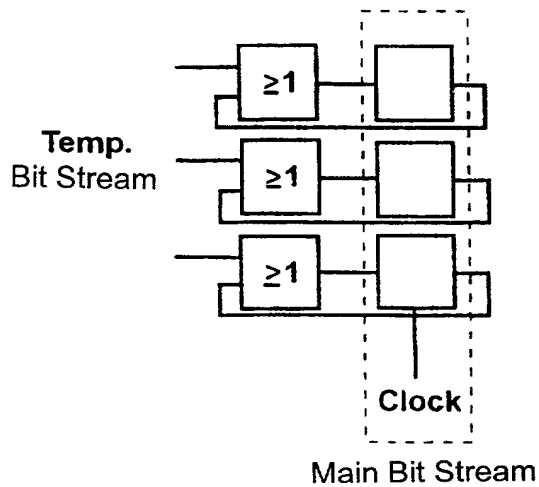


FIG 9

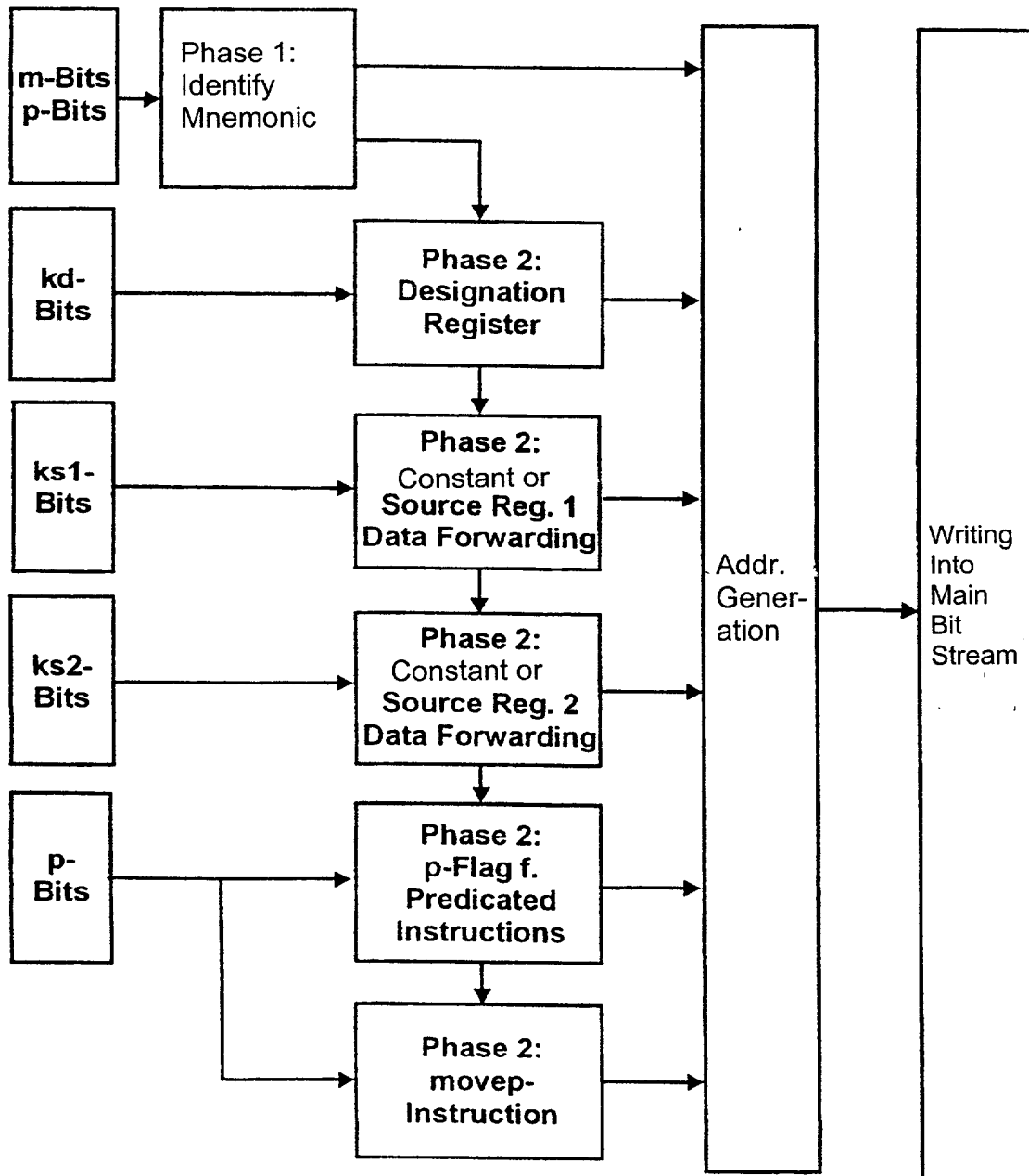


FIG 10

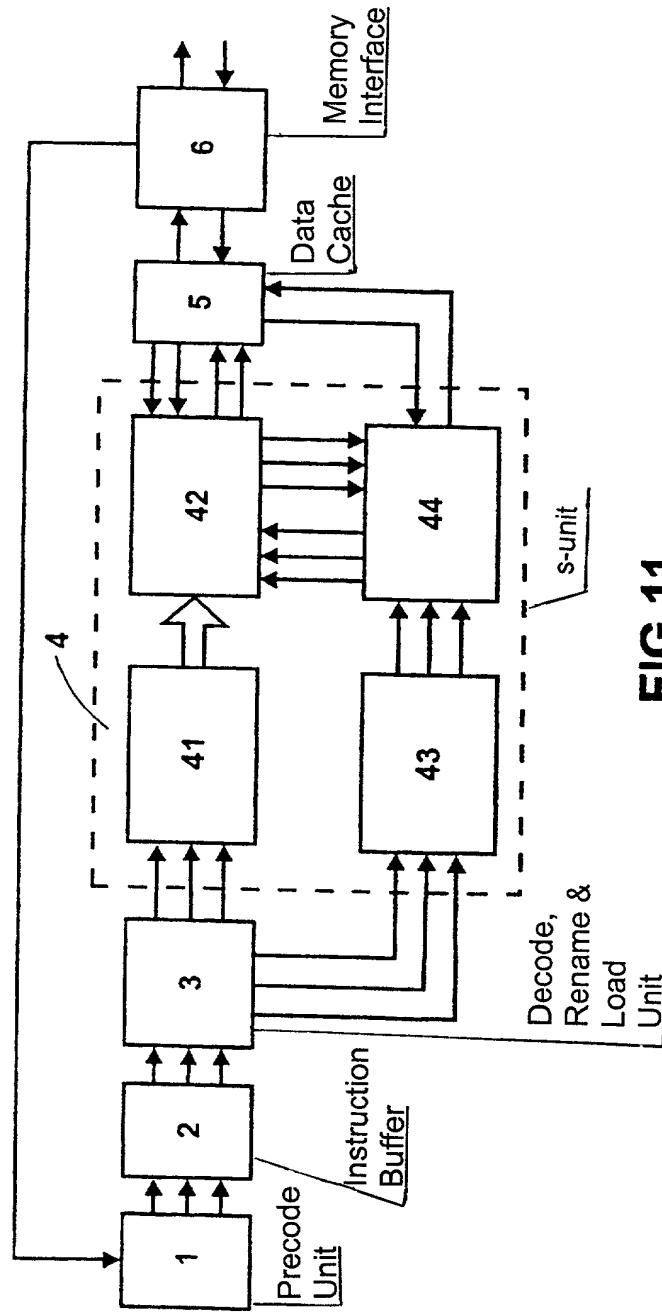


FIG 11

Prior Art

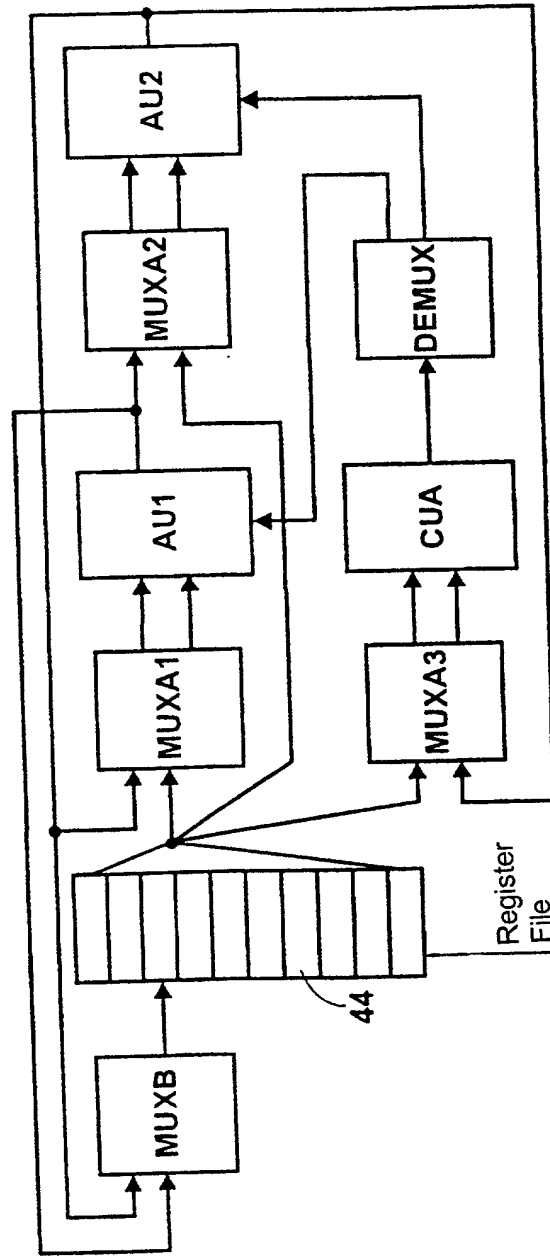


FIG 12